What is Claimed is:

1. A multiplier-accumulator block comprising:

a first multiplier used in implementing first mode of operation; and

a second multiplier used in simultaneously implementing a second mode of operation.

2. The multiplier-accumulator block of claim 1 further comprising an additional one or more multipliers used in implementing the first mode of operation.

3. The multiplier-accumulator block of claim 1 further comprising an additional one or more multipliers used in implementing the second mode of operation.

4. The multiplier-accumulator block of claim 1 wherein the first multiplier is an 18 bit by 18 bit multiplier and the second multiplier is an 18 bit by 18 bit multiplier, the multiplier-accumulator block further comprising two additional 18 bit by 18 bit multipliers.

5. The multiplier-accumulator block of claim 4 wherein the first mode is selected from the group consisting of: 18 bit by 18 bit multiply, 52 bits accumulate, initialize/zero accumulator, sum of 2 18 bit by 18 bit multiply, sum of 4 18 bit by 18 bit multiply, 9 bit by 9 bit multiply, sum of 2 9 bit by 9 bit multiply, sum of 4 9 bit by 9 bit multiply, and 36 bit by 36 bit multiply.

6. The multiplier-accumulator block of claim 1 further comprising a plurality of control signals used to indicate the first mode and the second mode.

7. The multiplier-accumulator block of claim 1 further comprising circuitry for adding, subtracting, and accumulating inputs.

8. The multiplier-accumulator block of claim 1 further comprising a third multiplier used in simultaneously implementing a third mode of operation.

9. A programmable logic device comprising the multiplier-accumulator block of claim 1.

10. A multiplier-accumulator block comprising:

four 18 bit by 18 bit multipliers arranged in two pairs;

a first arithmetic circuitry coupled to one of the pairs;

a second arithmetic circuitry coupled to another of the pairs; and

control circuitry coupled to the multipliers and the arithmetic circuitry, the control circuitry controls in which modes of operation the multiplier-accumulator is to operate, wherein the multiplier-accumulator is capable of operating in more than one mode of operation at one time.

11. The multiplier-accumulator block of claim 10 wherein the first arithmetic circuitry

comprises adder, subtracter, and accumulator circuitry and the second arithmetic circuitry comprises adder, subtracter, and accumulator circuitry.

12. The multiplier-accumulator block of claim 10 further comprising second stage arithmetic circuitry coupled to the first arithmetic circuitry and the second arithmetic circuitry.

13. The multiplier-accumulator block of claim 10 wherein the control circuitry comprises control signals.

14. The multiplier-accumulator block of claim 13 wherein the control signals comprise control signals for indicating that a particular one of the multipliers is to be configured to be used as two or more smaller multipliers.

15. The multiplier-accumulator block of claim 13 wherein the control signals comprise control signals for indicating that the outputs of a particular pair of the two pairs of multipliers are to be summed together.

16. The multiplier-accumulator block of claim 13 wherein the control signals comprise control signals for indicating that the outputs of the four multipliers are to be summed together.

17. The multiplier-accumulator block of claim 10 wherein the modes of operation are selected from the group consisting of: 18 bit by 18 bit multiply, 52 bits accumulate, initialize/zero accumulator, sum of 2 18 bit by 18 bit multiply, sum

of 4 18 bit by 18 bit multiply, 9 bit by 9 bit multiply, sum of 2 9 bit by 9 bit multiply, sum of 4 9 bit by 9 bit multiply, and 36 bit by 36 bit multiply.

18. A printed circuit board on which is mounted a programmable logic device as defined in claim 9.

19. The printed circuit board defined in claim 18 further comprising:

a memory mounted on the printed circuit board and coupled to the memory circuitry.

20. The printed circuit board defined in claim 19 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.